

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
14 July 2005 (14.07.2005)

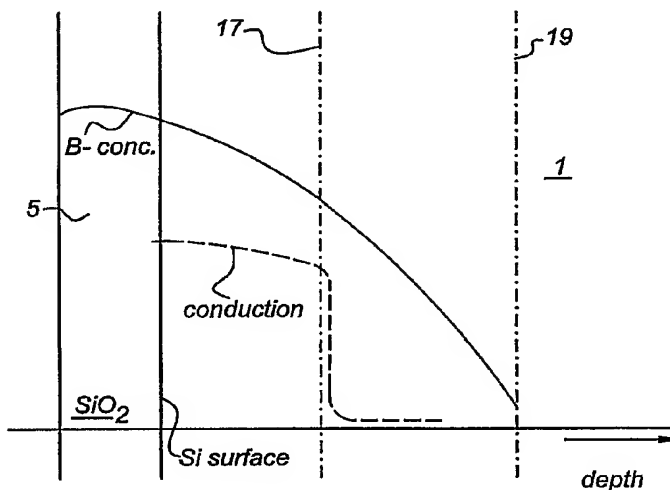
PCT

(10) International Publication Number  
**WO 2005/064662 A2**

- (51) International Patent Classification<sup>7</sup>: **H01L 21/265**, 21/336, 29/78, 21/00 (74) Agents: **ELEVELD, Koop, J.** et al.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (21) International Application Number: PCT/IB2004/052753 (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (22) International Filing Date: 10 December 2004 (10.12.2004) (81) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data: 03104871.3 22 December 2003 (22.12.2003) EP
- (71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): **PAWLAK, Bartlomiej, J.** [PL/BE]; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

[Continued on next page]

(54) Title: A SEMICONDUCTOR SUBSTRATE WITH SOLID PHASE EPITAXIAL REGROWTH WITH REDUCED DEPTH OF DOPING PROFILE AND METHOD OF PRODUCING SAME



(57) Abstract: Method of producing a semiconductor device, comprising: a) providing a semiconductor substrate, b) providing an insulating layer on a top surface of the semiconductor substrate, c) making an amorphous layer in a top layer of said semiconductor substrate by a suitable implant, d) implanting a dopant into said semiconductor substrate through said insulating layer to provide said amorphous layer with a predetermined doping profile, said implant being performed such that said doping profile has a peak value located within said insulating layer, e) applying a solid phase epitaxial regrowth action to regrow said amorphous layer and activate said dopant.

WO 2005/064662 A2



**Published:**

— without international search report and to be republished  
upon receipt of that report

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*